ABSTRACT OF THE DISCLOSURE

A FIFO memory includes a write counter for updating a write pointer in accordance with a write clock signal and a read counter for updating a read pointer in accordance with a read clock signal. A memory is connected to the write counter and the read counter and has memory cells. The memory performs a write operation for writing data to a memory cell corresponding to the write pointer and a read operation for reading data from a memory cell corresponding to the read pointer. A full flag control circuit generates a full flag synchronously with a write clock signal when the current read pointer and the next write pointer match. An empty flag control circuit generates an empty flag synchronously with a read clock signal when the current write pointer and the next read pointer match.